REMARKS

Claims 1 - 9 are pending in the present application.

In the Office Action, claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,893,072 to Matsumoto (herinafter "the Matsumoto patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent"). Applicants are respectfully traversing the rejection.

Claim 1 provides for a testing unit. The testing unit includes, *inter alia*, a signal generator, a receiving unit, and a synchronizing unit for synchronizing a data flow of a signal between a device under test (DUT) and the receiving unit. The synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit. The synchronization unit includes a buffer where a write access onto the buffer is controlled by the first clock signal, and a read access onto the buffer is controlled by the second clock signal.

The Office Action indicates that the Matsumoto patent discloses a receiving unit and a signal generator, and that the Alston patent discloses a synchronizing unit. Thus, the Office Action asserts that the Matsumoto and Alston patents, in combination, disclose the elements of claim 1. Below, Applicants explain that the cited combination of the Matsumoto and Alston patents is improper for purposes of a section 103(a) rejection of claim 1.

The Matsumoto patent is directed toward an apparatus for testing an integrated circuit (IC). The Matsumoto patent at col. 1, lines 44 – 51 states:

> In such an IC device, plural logic stages in the multi-stage logic circuit section successively transmit a signal under control of a clock signal, and thus a time delay shift of the signal associated with the period of the clock signal is generated. Hence, the delay time of the output data signal from the to-be-measured IC device is different from the delay time of the expected signal from the IC tester...(emphasis added)

Thus, the problem that the Matsumoto patent addresses is that a time delay shift causes different delay times between an output to-be-measured and an expected signal. The Matsumoto patent proposes compensating for the different delays by passing the expected signal through transferring circuits, the number of which is equal to the number of clocked logic circuits included in the logic circuit section of the IC device for transferring the test signal (col. 3, lines 29 – 33).

As shown in FIGS. 2 and 5 of the Matsumoto patent, (a) different signal timing delays are introduced by flip-flop circuits 30 – 32 (col. 4, lines 45 – 52), and (b) transferring circuits to compensate for the different delays are implemented by series combinations of flip-flop circuits F11 – Fnn (col. 4, lines 58 – 65). A specific example of the compensation is provided at col. 5, lines 8 – 16. Each of the flip-flop circuits 30 to 33 and F11 to Fnn is triggered by a timing signal from a timing signal generator TG, that is, is operated in control of clock pulses (col. 5, lines 21 – 24).

The Alston patent is directed toward a synchronization circuit for transferring data between two asynchronous circuits. As explained at col. 6, lines 10 – 16:

> [A] transmitting circuit 102 operates in synchronism with a first clock signal (CLOCK1) on a first clock signal line 106, and the receiving circuit 104 operates in synchronism with a second clock signal (CLOCK2) on a second clock signal line 108. The two clock signals operate asynchronously with respect to each other and may have substantially different frequencies. (emphasis added).

The Matsumoto, through implementation of flip-flop circuits F11 – Fnn, compensates for different delay times, and so purportedly solves the problem caused by different delay times. As such, the Matsumoto patent does not have any need for a synchronization circuit as disclosed by the Alston patent. Thus, Applicants submit that **there is no motive** for the cited combination of the Matsumoto and Alston patents.

Furthermore, a modification of the apparatus of the Matsumoto patent to include a synchronization circuit as disclosed by the Alston patent would apparently obviate the need for flip-flop circuits F11 – Fnn. Therefore, a modification of the Matsumoto patent to include the would **change the principle of operation** of the apparatus of the Mastsumoto patent.

Moreover, whereas in the Matsumoto patent all of the flip-flop circuits are triggered by a timing signal from a timing signal generator TG, the signals are synchronous with respect to one another. In contrast, as noted above, the clock signals in the Alston patent are asynchronous with respect to one another. Thus, the apparatus of the Matsumoto patent and the apparatus of the Alston patent are **technically non-analogous** to one another.

Applicants respectfully submit that:

(A) whereas the cited combination of the Matsumoto and Alston patents:

(i) lacks a motive, and

(ii) would change the principle of operation of the apparatus of the Mastsumoto patent, and

(B) whereas the apparatus of the Matsumoto patent and the apparatus of the Alston patent are technically non-analogous to one another,

the cited combination of the Matsumoto and Alston patents is improper for purposes of a section 103(a) rejection of claim 1. Therefore, claim 1 is patentable over the cited combination of references.

Claims 2 – 7 depend from claim 1. By virtue of this dependence, claims 2 – 7 are also patentable over the cited combination of references.

Claim 8 is an independent claim and includes recitals similar to those of claim 1, as described above. Thus, for reasoning similar to that provided in support for claim 1, Applicants submit that claim 8 is patentable over the cited combination of references.

Claim 9 depends from claim 8. By virtue of this dependence, claim 9 is also patentable over the cited combination of references.

In view of the foregoing, Applicants respectfully submit that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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